TITLE: SURGE CURRENT CHIP RESISTOR

BACKGROUND OF THE INVENTION

The present invention relates to chip resistors. More
particularly, the present invention relates to chip resistors
designed to tolerate high surge current.

In a number of applications, chip resistors are required
to dissipate pulsed electrical power. Such applications
include protective circuitry for communication lines, motor
drives, and power supplies. In these and other applications,
voltages are applied to the terminals of the resistor for
short time periods. Sometimes this is referred to as pulse
loading. This amount of time of each pulse is commonly less
than one second.

The general problem with using chip resistors in
applications and environments which involve pulse loading
relates to the magnitude of the instantaneous pulsed power.
The instantaneous pulsed power may be many times higher than
the steady state power rating of the resistor. When the
instantaneous power is great enough or applied for a long
enough time period, the result is resistor failure. Thus the
problem is to maximize the pulsed power that may be safely
dissipated by the resistor.

Various prior attempts at solving this problem have been
made. One such attempt applicable to thick film resistor
chips involves laser trimming. One example of laser trimming
a thick film resistor chip is found in U.S. Patent No.
5,874,887 to Kosinski. In the laser trimming of Kosinski,
special methods are used to smooth the electrical current
distribution in the resistive film through specially oriented
or positioned cuts. Another prior art attempt has involved
giving up on the use of laser cutting. One example of such a

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device is the SG73 Flat Chip Surge Current Thick Film resistor available from KOA.

Another approach has involved using special types of resistor pastes. Special resistor pastes are used to form restive film that is more tolerant to pulse loading as compared to the resistive film originating from a regular resistive paste. One example of the use of resistor pastes is disclosed in U.S. Patent No. 5,464,564 to Brown.

Despite these attempts, problems remain. Therefore, it is a primary object of the invention to improve upon the state of the art.

It is a further object of the present invention to provide a chip resistor that has improved tolerance for instantaneous pulsed power.

Another object of the present invention is to provide a chip resistor that has improved tolerance for instantaneous pulsed power without increasing the size of the chip.

Yet another object of the present invention is to provide a chip resistor that is not susceptible to solder joint fatigue caused by multiple pulse applications.

A further object of the present invention is to provide a chip resistor that is not limited to a particular manufacturing process and can be a thick-film resistor, thin-film resistor, or a foil resistor.

A still further object of the present invention is to provide a chip resistor that can be efficiently manufactured without substantially increasing manufacturing costs.

BRIEF SUMMARY OF THE INVENTION

The invention relates to a chip resistor capable of dissipating short duration, high level electrical power. The chip resistor of the present invention is applicable to all types of chip resistors having resistive layers attached to

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the much thicker substrate, including thick-film resistors, thin-film resistors, and foil resistors.

The chip resistor of the present invention includes a substrate having opposite parallel first and second surface. The first surface 24 and the second surface 26 are also symmetrical.

The chip resistor of the present invention further includes a first resistive layer and a second resistive layer. The first resistive layer and the second resistive layer are located symmetrically on both sides of the substrate. When electrical current passes through the resistive layers, a temperature distribution within the substrate will be substantially symmetrical about a central longitudinal plane of symmetry of the substrate for eliminating thermal bending. The central longitudinal plane of symmetry is defined by a cross section along a central longitudinal axis of symmetry. Resistor terminals electrically connect the first resistive layer and the second resistive layer in parallel.

The chip resistor of the present invention has been shown to provide a number of advantages over prior art chip resistors. In particular, the chip resistor of the present invention tolerates higher instantaneous pulsed power when compared to a same size prior art chip resistor. In addition, the chip resistor of the present invention is not susceptible to solder joint fatigue caused by the application of multiple pulses thus providing a substantial advantage over prior art due to a temperature distribution that is symmetrical about a middle plane and which eliminates thermal bending. Further, an additional manufacturing benefit of the present invention is that it may be directly loaded to a pick-and-place machine from a bulk case without concern for top-bottom orientation.

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BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a front view of a prior art chip resistor.

Figure 2 is a front view of a chip resistor according to the present invention.

DETAILED DESCRIPTION OF THE INVENTION

Figure 1 shows a side view of a prior art chip resistor 10. The prior art as shown in Figure 1 is characterized by a single resistive layer 12 which may be covered by a protective coating. The single resistive layer 12 is located on one side of a ceramic substrate 14. The chip resistor 10 also includes resistor terminals 16.

One embodiment of the present invention is shown in Figure 2. The chip resistor 20 of the present invention includes a first resistive layer 12 and a second resistive layer 22. Each of the resistive layers (12 and 22) may be covered by protective coatings (not shown). The first resistive layer 12 and the second resistive layer 22 are located symmetrically on both sides of the substrate 14 which may be a ceramic substrate. The resistor terminals 16 electrically connect the first resistive layer 12 and the second resistive layer 22 in parallel. The resistor terminals 16 are suitable for solder or adhesive or wire bond mounting to a circuit board.

A central longitudinal plane A-A (plane of symmetry) is shown transversing the chip resistor 20. The central longitudinal plane of symmetry is defined as the plane defined by a cross section along a central longitudinal axis of symmetry. The longitudinal plane A-A is substantially parallel to a first surface 24 of the substrate 14 and a second surface 26 of the substrate 14. The central longitudinal plane A-A is substantially equidistant between

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the first surface 24 and the second surface 26. The substrate has a rectangular cross-section (not shown). Preferably, the first resistive layer 12 and the second resistive layer 22 are symmetric about the central longitudinal plane.

The chip resistor 20 of Figure 2 has been shown to provide a number of advantages over prior art chip resistors. In particular, chip resistor 20 tolerates higher instantaneous pulsed power when compared to a same size prior art chip resistor. In particular, this increased tolerance can be up to two times as high depending upon the pulse duration.

The chip resistor of the present invention also is not susceptible to solder joint fatigue caused by the application of multiple pulses thus providing a substantial advantage over prior art. In particular, the chip resistor 20 has a temperature distribution substantially symmetrical about the central longitudinal plane for eliminating thermal bending.

Further, an additional manufacturing benefit of the present invention is that it may be directly loaded to a pick-and-place machine from a bulk case without concern for top-bottom orientation.

Dissipation of the pulsed power in the chip resistor may be regarded as short-time heat generation in the resistive layer attached to the substrate surface and simultaneous heat transfer into the substrate. It is noted that heat transfer outside the resistor during short-time pulse application is generally considered negligible. The overload of the resistor by single or multiple pulses may result in resistor failure. Types of resistor failure includes resistive layer burn-off and solder joint fatigue.

If the voltage applied to the resistor does not exceed the maximum permissible voltage the resistor failure commonly

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stems from overheating of the resistive layer. It may be
shown analytically that the maximum temperature rise in the
resistive layer is proportional to the applied electrical
power and inversely proportional to the resistive layer area:

$$T(t) = \frac{2W}{S} \cdot \sqrt{\frac{t}{\pi k c \rho}} \qquad (1)$$

where:

t - time, sec;

T(t) - temperature rise in the resistive film, K;

W - square-wave pulse power, W;

S - resistive layer area, m^2;

π = 3.14;

k - thermal conductivity of the substrate material, W/(m·K);

c - heat capacity of the substrate material, J/(kg·K);

ρ - density of the substrate material, kg/m^3.

The additional resistive layer 22 in the resistor 20
doubles the total resistive layer area as compared to that of
Figure 1. Therefore double power applied to the proposed
resistor will result in the same temperature rise in its
resistive layer as in the case of one-fold power application
to the prior art chip resistor of the same substrate size.

This effect may be explained in the different way. The
electrical current that passes through the resistor 20
divides, and half of it passes through the upper resistive
layer 12 while the second half passes through the lower
resistive layer 22. The density of the current, power, and
temperature rise in each resistive layer will be half of that
in the prior art chip resistor of the same substrate size
loaded by the same pulse load (i.e. Figure 1). Therefore,
the maximal pulsed power dissipated by the chip resistor

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according to the present invention is as large as
approximately twice that of a prior art chip resistor of the
same substrate size.

The described effect takes place only in the case of the
short-time loading when pulse duration does not exceed the
characteristic time needed for heat propagation through the
substrate that separates two resistive layers in the proposed
chip resistor. The mentioned characteristic time depends on
the thickness and physical properties of the substrate:

$$\tau = \frac{c\rho h^2}{4k} \qquad\qquad (2)$$

Where τ is characteristic time expressed in seconds, h is the
substrate thickness expressed in meters, the other parameters
are the same as in equation (1). For example, for 0.5 mm
alumina substrate $\tau \approx 10$ milliseconds. That means that the
doubled power capacity will be relevant to 0 - 10
milliseconds range of pulse duration. The further extension
of pulse duration gradually reduces the pulsed power capacity
of the proposed resistor to the pulsed power capacity of
prior art resistor.

Another type of resistor failure involves solder joint
fatigue. It may be shown that prior art chip resistor loaded
by pulse is characterized by monotone decreasing temperature
distribution in direction from resistive layer to the
opposite free surface of the substrate. This temperature
distribution results in monotone decreasing of thermal
expansion of the substrate in the same direction. It becomes
apparent in the substrate bending. The bending creates
mechanical stress in the solder joints between the chip and
printed circuit board. Multiple application of the pulses
may result in solder joint fatigue (cracking).

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The chip resistor of the present invention has symmetrical construction as shown in Figure 2. Its temperature distribution is non-uniform but symmetrical with respect to the central longitudinal plane A-A. The symmetry completely eliminates thermal bending of the chip and the damage of the solder joints resulting from the multiple pulse loading.

The chip resistor of the present invention is not limited to a particular type of resistor, but rather applies to any number of types of resistors including thick-film resistors, thin-film resistors, and foil resistors.

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